What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a plurality of cell blocks provided on the semiconductor substrate;

a plurality of gate electrodes electrically independent of one another and respectively provided in the plurality of cell blocks; and

a plurality of gate pads provided on the semiconductor substrate and respectively connected with the plurality of gate electrodes.

2. The semiconductor device according to claim 1, wherein:

the semiconductor substrate has a rectangular shape; and

the plurality of gate pads are arranged at a side portion of the semiconductor substrate.

3. The semiconductor device according to claim 1, further comprising:

a ground terminal provided outside of the semiconductor substrate and grounded; and

a gate terminal provided outside of the semiconductor substrate and electrically independent of the ground terminal, wherein:

the plurality of cell blocks includes a first cell block that is non-defective, and a second cell block that is defective; and

the plurality of gate pads includes a first gate pad connecting the first cell block to the gate terminal, and a second gate pad connecting the second cell block to the ground terminal.

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4. The semiconductor device according to claim 3, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is boned to the ground terminal by one of wire-bonding, soldering, and pressure welding.

5. The semiconductor device according to claim 1, further comprising:

a gate terminal provided outside of the semiconductor substrate;

an emitter pad provided on the semiconductor substrate to have an emitter potential; and

a source pad provided on the semiconductor substrate to have a source potential, wherein:

the plurality of cell blocks includes a first cell block that is non-defective, and a second cell block that is defective; and

the plurality of gate pads includes a first gate pad connecting the first cell block to the gate terminal, and a second gate pad connecting the second cell block to one of the emitter pad and the source pad.

6. The semiconductor device according to claim 4, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the one of the emitter pad and the source pad by one of wire-bonding, soldering, and pressure-welding.

7. The semiconductor device according to claim 1, wherein the semiconductor substrate is an insulated gate type bipolar transistor chip.

8. The semiconductor device according to claim 1, further comprising a plurality of marks provided at a plurality of regions of the semiconductor substrate, respectively corresponding to the plurality of cell blocks, each of the marks being for discriminating whether a corresponding one of the cell blocks is defective.

9. The semiconductor device according to claim 8, wherein discrimination of whether each of the cell blocks is defective is determined by at least one of a location, a color, a size, and a shape of a corresponding one of the marks on the semiconductor substrate.

10. The semiconductor device according to claim 8, wherein discrimination of whether each of the cell blocks is defective is determined by a number of the marks corresponding to the each of the cell blocks.

11. The semiconductor device according to claim 8, wherein:

the plurality of cell blocks include a first cell block;

the plurality of gat pads include a first gate pad connected with the first cell block; and

the plurality of marks includes a first mark for discriminating whether the first cell block is defective, the first mark being provided on a line passing through the first gate pad.

12. The semiconductor device according to claim 11, wherein the first mark is provided at a side of the first gate pad opposite to the first cell block.

13. The semiconductor device according to claim 11, wherein:

the plurality of cell blocks include a second cell block;

the plurality of gate pads include a second gate pad connected with the second cell block;

the plurality of marks include a second mark for discriminating whether the second cell block is defective, the second mark being provided out of a line passing through a center of the second gate pad;

first one of the first cell block and the second cell block is defective; and

second one of the first cell block and the second cell block

is non-defective.

14. The semiconductor device according to claim 8, wherein each of the plurality of marks is provided is at a vicinal region of a corresponding gate pad or on a surface of the corresponding gate pad.

15. The semiconductor device according to claim 8, wherein the plurality of marks can be recognized by an image recognition device of a wire-bonding apparatus.

16. The semiconductor device according to claim 1, further comprising a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacently to the plurality of gate pads.

17. The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor substrate, wherein:

the plurality of cell blocks includes a first cell block and a second cell block, the first cell block being non-defective and connected with the gate terminal, the second cell block being defective and connected with one of the plurality of pads.

18. The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided

in the plurality of cell block;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes;

a collector electrode provided on a back surface of the semiconductor substrate;

an emitter terminal bonded to the main surface of the semiconductor substrate and electrically connected with the plurality of emitter pads;

a collector terminal bonded to the back surface of the semiconductor substrate and electrically connected with the collector electrode; and

a resin member encapsulating the gate terminal, the emitter terminal, and the collector terminal together.

19. The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads electrodes provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes; and

an emitter terminal provided outside of the semiconductor substrate and electrically connected with the emitter pads, wherein:

the first cell block is connected to the gate pad through a first bonding wire; and

the second cell block is connected to the one of the plurality of pads through a second bonding wire.

20. The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor device, wherein:

the plurality of cell blocks includes a first group of cell blocks having an equal threshold voltage and connected with the gate terminal, and a second group of cell blocks having different threshold voltages from one another and connected with one of the plurality of pads.

21. A method for manufacturing a semiconductor device, comprising:

preparing a semiconductor substrate having a plurality of cell blocks thereon, a plurality of gate electrodes respectively provided in the cell blocks and electrically independent of one another, and a plurality of gate pads respectively connected with the plurality of gate electrodes; and

forming a plurality of marks at a plurality of regions on the semiconductor substrate corresponding to the plurality of cell blocks respectively for discriminating whether the plurality of cell blocks are defective.

22. The method according to claim 21, wherein the plurality of marks are formed on the semiconductor substrate with ink by printing or coating.

23. The method according to claim 21, further comprising:

determining whether one of the cell blocks is defective based on a corresponding mark;

wire-bonding the one of the cell blocks to a first terminal when the one of the cell blocks is determined as a defective one, and to a second terminal when the one of the cell blocks is determined as a non-defective one by the mark, the first terminal being electrically independent of the second terminal.

24. The method according to claim 23, wherein the mark is recognized as an image recognition machine for determining whether the one of the cell blocks is defective.

25. The method according to claim 24, wherein:

when the plurality of marks are formed, if a first one of the cell blocks is defective, a first mark corresponding to the first one is formed at a vicinal region of the first one, and if a second one of the cell blocks is non-defective, a second mark corresponding to the second one is formed at a vicinal region of the second one; and

at least one of a size, color, a shape, and a number of the first mark is different from that of the second mark.

26. A method for manufacturing a semiconductor device, comprising:

preparing a semiconductor substrate having a plurality of

cell blocks thereon, a plurality of gate electrodes respectively provided in the cell blocks and electrically independent of one another, a plurality of gate pads respectively connected with the plurality of gate electrodes, a plurality of emitter electrodes respectively provided in the cell blocks on the semiconductor substrate, and a plurality of emitter pads respectively connected with the plurality of emitter electrodes; and

determining whether one of the cell blocks is defective using a corresponding one of the gate pads and a corresponding one of the emitter pads.

27. The method according to claim 26, wherein the determination of whether the one of the plurality of cell blocks is defective is made based on a withstand voltage between the corresponding one of the gate pads and the corresponding one of the emitter pads.

28. The method according to claim 26, further comprising:

wire-bonding the corresponding one of the gate pads to a gate terminal provided outside of the semiconductor substrate if the one of the plurality of cell blocks is non-defective, and to the corresponding one of the emitter pads or a ground terminal having a ground potential if the one of the plurality of cell blocks is defective.

29. The method according to claim 26, further comprising forming a plurality of marks on the semiconductor substrate for

discriminating whether the plurality of cell blocks are defective.

30. A method for manufacturing an insulated gate type power IC, comprising:

preparing a plurality of chips, each of the plurality of chips having a semiconductor substrate, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes respectively provided in the cell blocks and electrically independent of one another, and a plurality of gate pads respectively connected with the plurality of gate electrodes;

sorting the plurality of chips such that a group of chips, each having a defective cell block at an identical arrangement position, gather exclusively, wherein:

the defective cell block in each chip has a corresponding gate electrode that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential; and

a non-defective cell block in the each chip has a corresponding gate electrode that is connected with a gate terminal provided outside of the semiconductor substrate.

31. The method according to claim 30, wherein the plurality of chips are sorted and selectively held in a plurality of trays of a chip transfer machine.

32. The method according to claim 31, wherein the arrangement position of the defective cell is measured by a wafer

acceptance test (WAT) as chip information and is transmitted to the chip transfer machine.

33. The method according to claim 31, wherein the chip transfer machine measures the arrangement position of the defective cell as chip information.

34. The method according to claim 30, wherein chip information for sorting the plurality of chips contains at least one of a threshold voltage, a voltage between a collector electrode and an emitter electrode, and switching characteristics, in addition to the arrangement position of the defective cell block.

35. The method according to claim 34, wherein the plurality of chips are sorted and selectively held in a plurality of trays of a chip transfer machine based on the chip information.

36. The method according to claim 35, wherein the chip information for each chip is measured by a wafer acceptance test (WAT) and is transmitted to the chip transfer machine.

37. The method according to claim 35, wherein the chip transfer machine measures the chip information for soaring the plurality of chips.

38. An apparatus for manufacturing an insulated gate type power IC, comprising:

a chip transfer machine including a plurality of trays for selectively holding a plurality of chips, each of which has a semiconductor substrate, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes respectively provided in the cell blocks and electrically independent of one another, and a plurality of gate pads respectively connected with the gate electrodes, wherein:

the plurality of chips being sorted based on an arrangement position of a defective cell of each cell to be selectively held by the plurality of trays;

the defective cell has a corresponding gate pad that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential; and

a non-defective cell of each cell has a corresponding gate pad that is connected with a gate terminal provided outside of the semiconductor substrate.

39. An insulated gate type power IC module, comprising a plurality of insulated gate type ICs, each of the plurality of insulated gate type ICs comprising:

a semiconductor substrate;

a plurality of cell blocks provided on the semiconductor substrate;

a plurality of gate electrodes respectively provided in the plurality of cell blocks and electrically independent of one another; and

a plurality of gate pads respectively connected wit the

plurality of gate electrodes, wherein:

each of the insulated gate type ICs includes a defective cell block at an identical position, and a non-defective cell block, the defective cell block having a corresponding gate electrode that is connected with one of a ground terminal provided outside of the semiconductor substrate and an emitter pad provided on the semiconductor substrate, the non-defective cell block having a corresponding gate electrode that is connected with a gate terminal provided outside of the semiconductor substrate; and

the insulated gate type power IC module is composed of the plurality of insulated gate type ICs exclusively.

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